UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,324	08/27/2001	Robert T. George	2207/12003	5090

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EXAMINER
KIM, HONG CHONG

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *10 July 2006*.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-17* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-17* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a) ☐ All   b) ☐ Some * c) ☐ None of:

   1. ☐ Certified copies of the priority documents have been received.

   2. ☐ Certified copies of the priority documents have been received in Application No. _____.

   3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Detailed Action

1.   Claims 1-17 are presented for examination.   This office action is in response to

the amendment filed on 7/10/06.

Information Disclosure Statement

2.   Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3.   Claim 1-4, 6-12 and are rejected under 35 U.S.C. 103(a) as being unpatentable

over Shen et al. (Shen) U.S. Patent 6,526,481 in view of Rhodes U.S. Patent 6,859,861.

As to claim 1, Shen discloses a cache-coherent I/O device (Fig. 2 since each

cache is I/Oed by Refs. 110) comprising: a plurality of client port (Fig. 2 Refs. Refs.

130's), each to be coupled to one of a plurality of port components (Fig. 2 Refs. 110); a

cache (Fig. 2 Ref. 134), each coupled to one of said plurality of client ports and

assigned to one of said plurality of port components; and a coherency engine (Fig. 2

Refs. 132 & 140) coupled to said cache. However, Shen dos not specifically disclose a

plurality of sub unit caches.

However, it is well known in the cache art to divide a cache to a plurality of sub

unit caches. For example, Rhodes discloses a plurality of sub unit caches (Fig. 3) for

the purpose of expedite information access and thereby speed up the operation of the

computer system (col. 1 lines 23-30).

Accordingly, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to modify a cache unit of Shen into a plurality of sub

unit caches as disclosed in Rhodes for the advantages stated above.

As to claim 2, Shen and Rhodes disclose the invention as claimed in the above.

Shen further discloses wherein said plurality of port components includes processor port

components (Fig. 2 Ref. 110).

As to claim 3, Shen and Rhodes disclose the invention as claimed in the above.

Shen further discloses wherein said plurality of port components includes input/output

components (Fig. 2 Ref. 110).

As to claim 4, Shen and Rhodes disclose the invention as claimed in the above.

Shen further discloses wherein said plurality of sub-unit caches includes transaction

buffers using a coherency logic protocol (Fig. 2 Refs. 132 & 140).

As to claim 6, Shen discloses a cache-processing system comprising (Fig. 2): a

processor (Fig. 2 Ref 110); a plurality of port components (Fig. 2 Ref. 110); and a

cache-coherent I/O device (Fig. 2 Refs. 132 & 140) coupled to said processor and

including a plurality of client ports (Fig. 2 Ref. 130), each coupled to one of said plurality

of port components (Fig. 2 Ref. 110), said cache-coherent device further including a

cache (Fig. 2 Ref. 134), each coupled to one of said plurality of client ports and

assigned to one of said plurality of port components, and a coherency engine (Fig. 2

Fig. 140) coupled to said cache. However, Shen does not specifically disclose a

plurality of caches.

However, it is well known in the cache art to divide a cache to a plurality of

caches. For example, Rhodes discloses a plurality of caches (Fig. 3) for the purpose of

expedite information access and thereby speed up the operation of the computer

system (col. 1 lines 23-30).

Accordingly, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to modify a cache unit of Shen into a plurality of

caches as disclosed in Rhodes for the advantages stated above.

As to claim 7, Shen and Rhodes disclose the invention as claimed in the above.

Shen further discloses wherein said plurality of port components includes processor port

components (Fig. 1 Ref. 110).

As to claim 8, Shen and Rhodes disclose the invention as claimed in the above. Shen further discloses wherein said plurality of port components includes input/output components (Fig. 1 Ref. Ref. 110).

As to claim 9, Shen discloses the invention as claimed. Shen discloses in a cache-coherent I/O device (Fig. 2) including a coherency engine (Fig. 2 Refs. 132 & 140) and a plurality of client ports (Fig. 2 Refs 130), a method for processing a transaction, comprising: receiving a transaction request (col. 7 lines 13-15) at one of said plurality of client ports on the I/O cache-coherent device, said transaction request includes an address (col. 8 line 49); and determining whether said address is present (col. 8 lines 45+) in a cache (Fig. 2 Ref. 134), each of said cache assigned to said one of said plurality of client ports (Fig. 2 Ref. 110). However, Shen dos not specifically disclose a plurality of sub unit caches.

However, it is well known in the cache art to divide a cache to a plurality of sub unit caches. For example, Rhodes discloses a plurality of sub unit caches (Fig. 3) for the purpose of expedite information access and thereby speed up the operation of the computer system (col. 1 lines 23-30).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify a cache unit of Shen into a plurality of sub unit caches as disclosed in Rhodes for the advantages stated above.

As to claim 10, Shen and Rhodes disclose the invention as claimed in the above.
Shen further discloses wherein said transaction request is a read transaction request
(col. 7 lines 13-15).

As to claim 11, Shen and Rhodes disclose the invention as claimed in the above.
Shen further discloses transmitting data for said read transaction request from said one
of said plurality of sub-unit caches to one of said plurality of client ports (col. 8 lines
45+).

As to claim 12, Shen and Rhodes disclose the invention as claimed in the above.
Shen further discloses prefetching one or more cache lines ahead of said read
transaction request (cache memory reads on this limitation since the cache memory is
used to assure that the currently useful data of main memory are copied into the small
and fast cache for the purpose of increasing data access speed by means of spatial and
temporal localities); and updating the coherency state (Col. 9 lines 5-6) information in
said plurality of sub-unit caches.

As to claim 14, Shen and Rhodes disclose the invention as claimed in the above.
Shen further discloses wherein said transaction request is a write transaction request
(col. 7 lines 13-15).

4.   Claims 5, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Shen et al. (Shen) U.S. Patent 6,526,481 in view of Rhodes U.S. Patent 6,859,861

and further in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35,

1993, pp 140-240.

As to claims 5 and 13, Shen and Rhodes disclose the invention as claimed

above. However, neither Shen nor Rhodes specifically discloses wherein said

coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache

coherency protocol.

However, it is well known in the cache art to using MESI cache coherency

protocol for the purpose of maintaining data consistency thereby increasing the memory

access speed.   For example, Handy discloses coherency logic protocol includes a

Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

Accordingly, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to add coherency logic protocol includes a Modified-

Exclusive-Shared-Invalid (MESI) cache coherency protocol of Handy into the combined

invention of Shen and Rhodes for the advantages stated above.

As to claim 15, Shen, Rhodes, and Handy disclose the invention as claimed in

the above. Handy further discloses modifying coherency state information for a cache

line in said one of said plurality of sub-unit caches; updating coherency state information

in others of said plurality of sub-unit caches by said coherency engine; and transmitting

data for said write transaction request from said one of said plurality of sub-unit caches

to memory (MESI protocol reads on this limitation and pages 159-161).

5.   Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Shen et al. (Shen) U.S. Patent 6,526,481 in view of Rhodes U.S. Patent 6,859,861 and

Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp 140-240 and

further in view of Witt et al. (Witt) U.S. Patent 6,202,139.

As to claim 16, Shen further discloses modifying coherency state information of

said write transaction request (col. 7 line 13-15), however, neither Shen, Rhodes nor

Handy specifically discloses write transaction request in the order received and

pipelining multiple write requests.

Witt discloses write transaction request in the order received and pipelining

multiple write requests (col. 2 lines 42-43) for the purpose of avoiding bank conflicts

thereby decreasing the performance losses and increasing the access speed (col. 2

lines 43-45).

Therefore, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to incorporate write transaction request in the order

received and pipelining multiple write requests as shown in Witt into the combined

invention of Shen, Rhodes, and Handy because it would avoid bank conflicts thereby

decreasing the performance losses and increasing the access speed.

As to claim 17, Shen, Rhodes, Handy and Witt disclose the invention as claimed

in the above. Handy further discloses wherein the coherency state information includes

a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

Response to Arguments

6.   Applicant's arguments filed 7/10/06 have been fully considered but they are not

persuasive.

In response to applicant's argument on page 2 that the prior arts do not disclose

a cache coherent I/O device has been fully considered but it is not persuasive.

Shen discloses a cache-coherent I/O device (Fig. 2 since each cache is I/Oed by

Refs. 110 and a coherency is controlled by Refs. 140 and 132)   Also applicant states in

the instant application that "An input/output (I/O) device may also be utilized as a

caching I/O device" (block 6) is well known in the memory art. Applicant also states

that "a cache coherency protocol " (block 4) is well known in the memory art to

synchronize data in a plurality of caches.   In other words, the cache coherent I/O

device is well known in the memory art at the time the application was filed.

Therefore broadly written claims are disclosed by the references cited.

Conclusion

1.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

2.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

3.   When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show

how the amendments avoid such references or objections.   See 37 C.F.R. ' 1.111(c).

4.   When responding to the office action, Applicants are advised to provide the

examiner with the line numbers and page numbers in the application and/or references

cited to assist examiner to locate the appropriate paragraphs.

5.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Hong Kim whose telephone number is (571) 272-4181.

The examiner can normally be reached on M-F 9:00 to 6:00.

      If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim can be reached on (571) 272-4182. Any inquiry of a general

nature or relating to the status of this application should be directed to the TC 2100 .

whose telephone number is (571) 272-2100.

6.   Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

7.   Any response to this action should be mailed to:

                    Commissioner of Patents
                    P.O. Box 1450
                    Alexandria, VA 22313-1450

                    or faxed to TC-2100:
                    (571)-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim
Primary Patent Examiner
August 1, 2006